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(54) **ADAPTIVE FREQUENCY-DOMAIN REFERENCE NOISE CANCELLER FOR MULTICARRIER COMMUNICATIONS SYSTEMS**

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See application file for complete search history.

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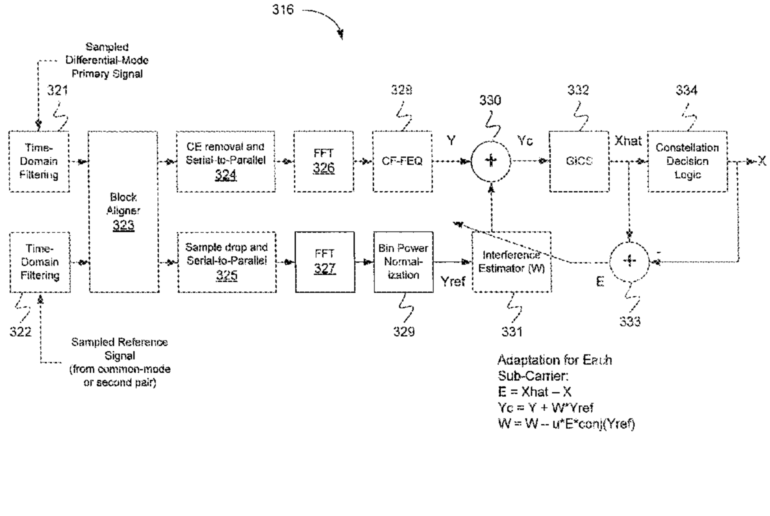
(57) **ABSTRACT**

A method and apparatus to align data blocks in a data signal and a reference signal to increase cross-correlation between the data signal and the reference signal as compared to the unaligned data and reference signals and cancel interference in the data signal in the frequency-domain under changing conditions and in the presence of the data signal.

20 Claims, 8 Drawing Sheets



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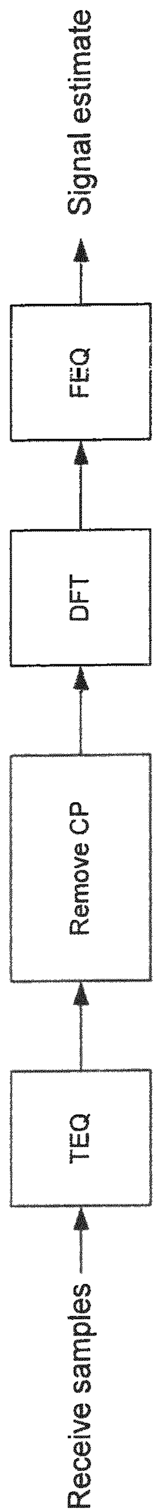


Figure 1

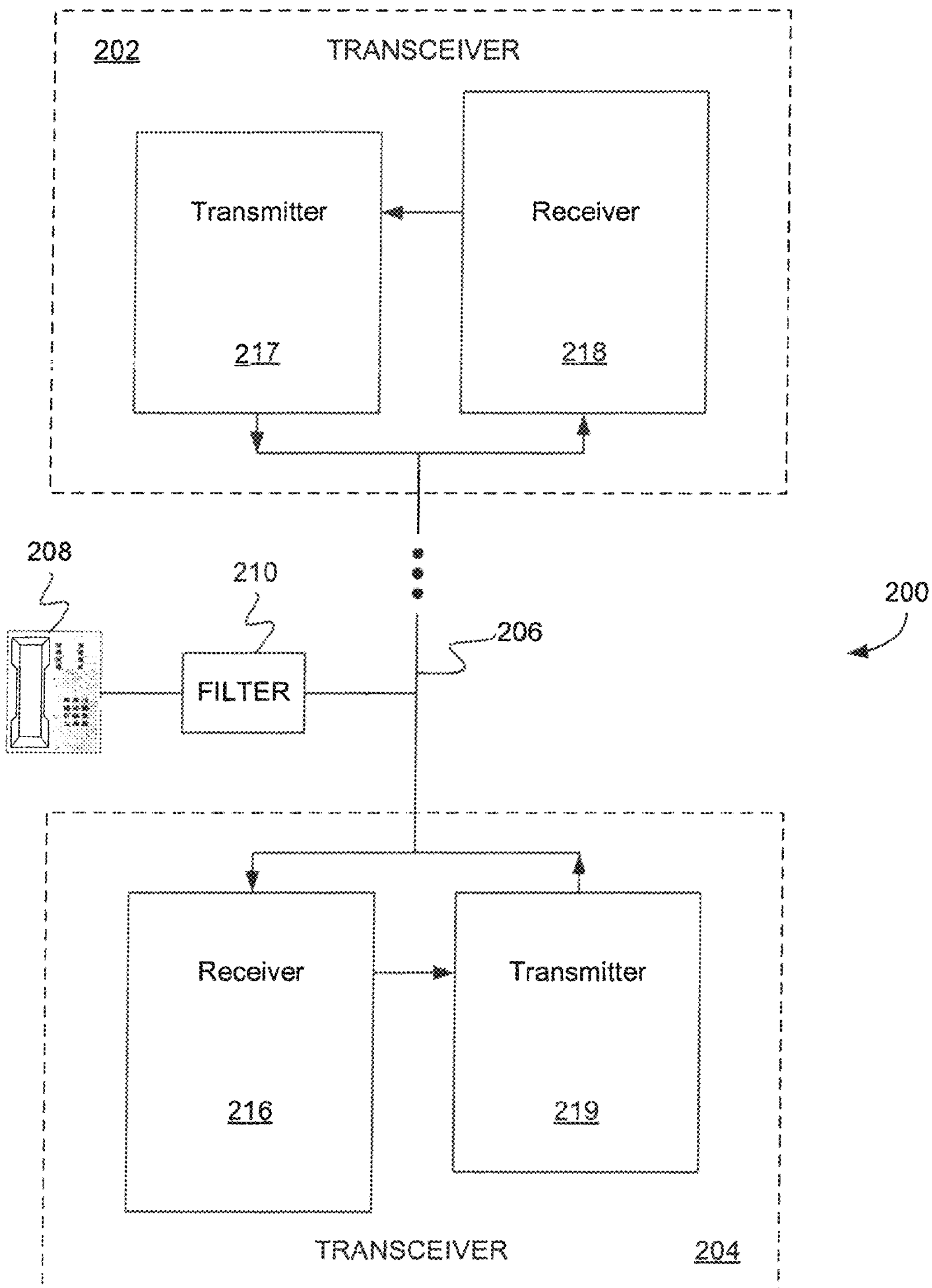
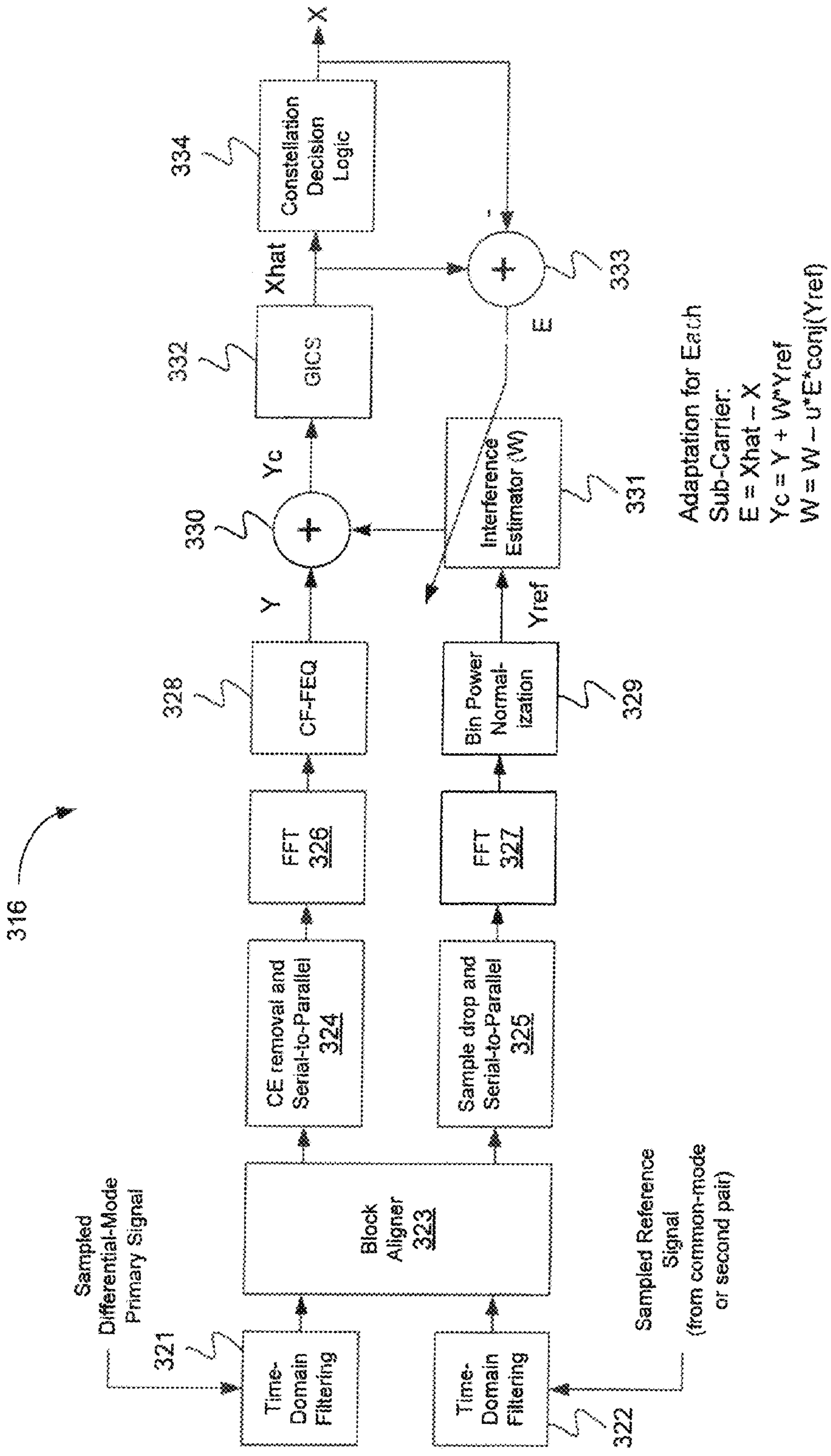

202
TRANSCEIVER
Transmitter
217
Receiver
218
208
210
FILTER
206
200
Receiver
216
Transmitter
219
TRANSCEIVER
204

Figure 2



316
Sampled Differential-Mode Primary Signal
321
Time-Domain Filtering
322
Time-Domain Filtering
Sampled Reference Signal (from common-mode or second pair)
Block Aligner 323
CE removal and Serial-to-Parallel 324
Sample drop and Serial-to-Parallel 325
FFT 326
FFT 327
328
CF-FEQ
329
Bin Power Normal-ization
Y
Yref
330
331
Interference Estimator (W)
Yc
332
GICS
Xhat
333
E
334
Constellation Decision Logic
X
Adaptation for Each Sub-Carrier:
E = Xhat – X
Yc = Y + W*Yref
W = W – u*E*conj(Yref)

Figure 3

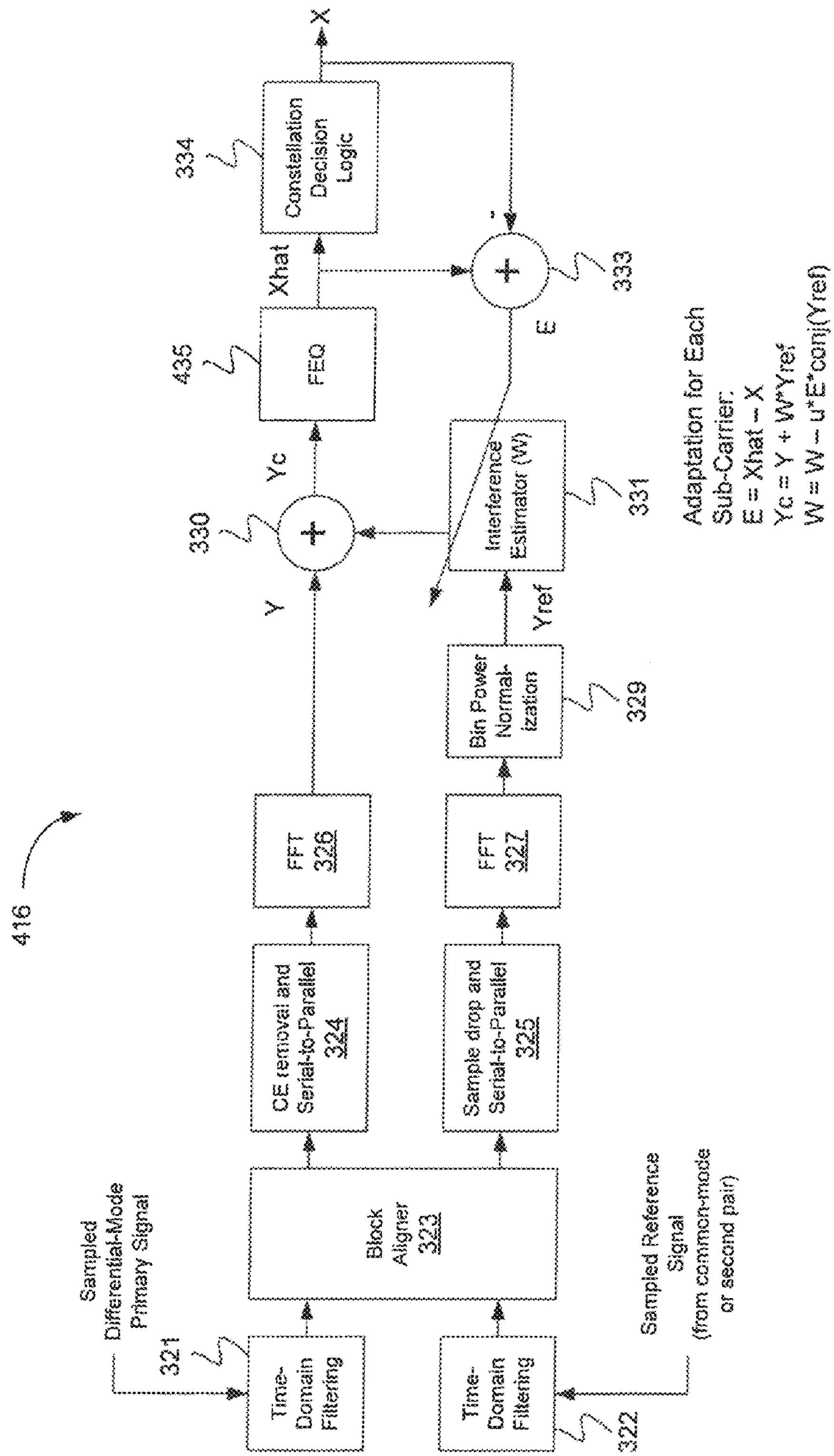

416
Sampled Differential-Mode Primary Signal
321
Time-Domain Filtering
Sampled Reference Signal (from common-mode or second pair)
322
Time-Domain Filtering
Block Aligner 323
CE removal and Serial-to-Parallel 324
Sample drop and Serial-to-Parallel 325
FFT 326
FFT 327
Bin Power Normal-ization
329
Y
Yref
330
Interference Estimator (W)
331
Yc
FEQ
435
Xhat
Constellation Decision Logic
334
X
333
E
Adaptation for Each Sub-Carrier:
E = Xhat – X
Yc = Y + W*Yref
W = W – u*E*conj(Yref)

Figure 4

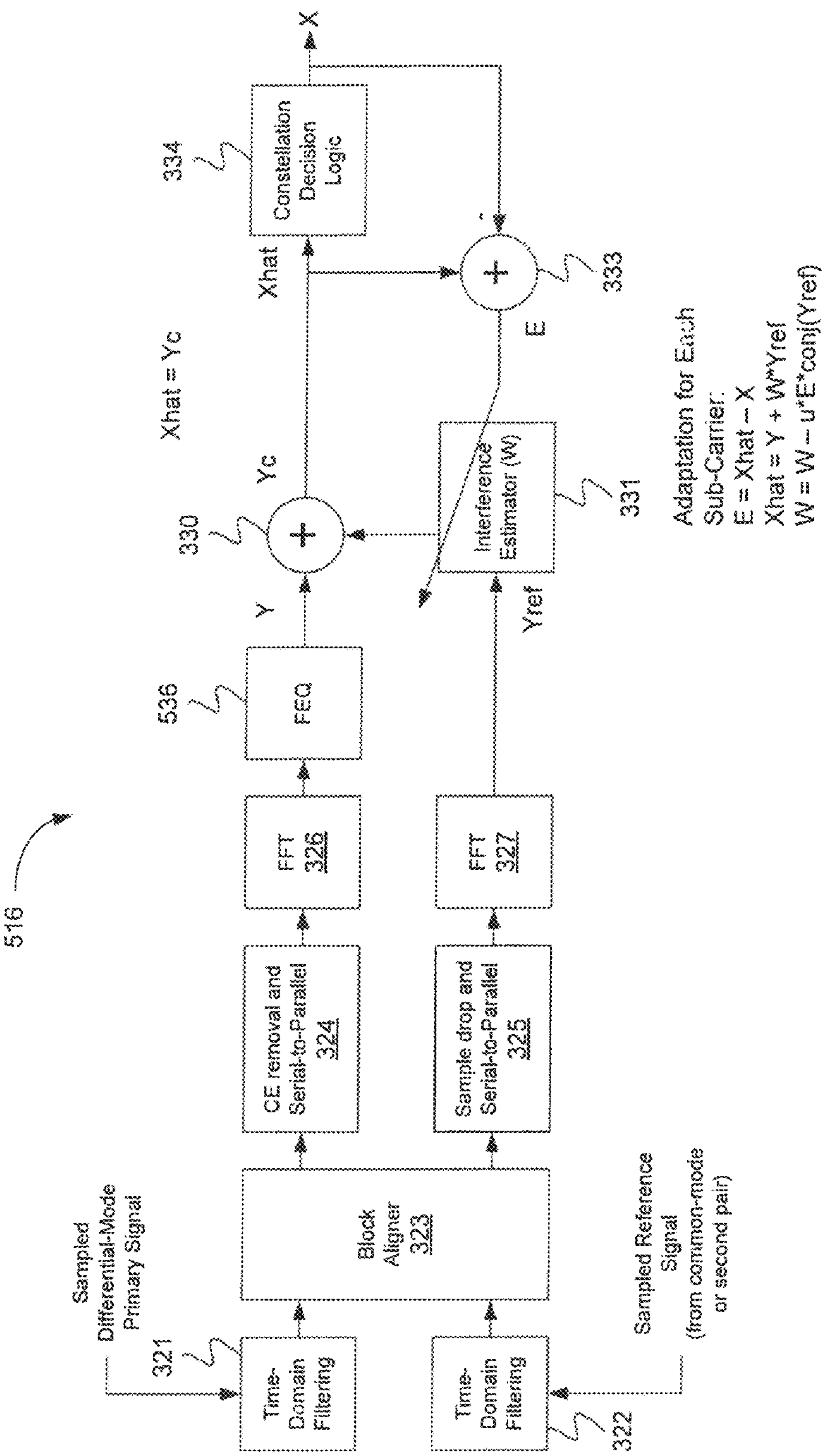

516
Sampled Differential-Mode Primary Signal
321
Time-Domain Filtering
Sampled Reference Signal (from common-mode or second pair)
322
Time-Domain Filtering
Block Aligner 323
CE removal and Serial-to-Parallel 324
Sample drop and Serial-to-Parallel 325
FFT 326
FFT 327
536
FEQ
Y
Yref
330
Yc
Xhat = Yc
Interference Estimator (W)
331
Xhat
333
E
334
Constellation Decision Logic
X
Adaptation for Each Sub-Carrier:
E = Xhat – X
Xhat = Y + W*Yref
W = W – u*E*conj(Yref)

Figure 5

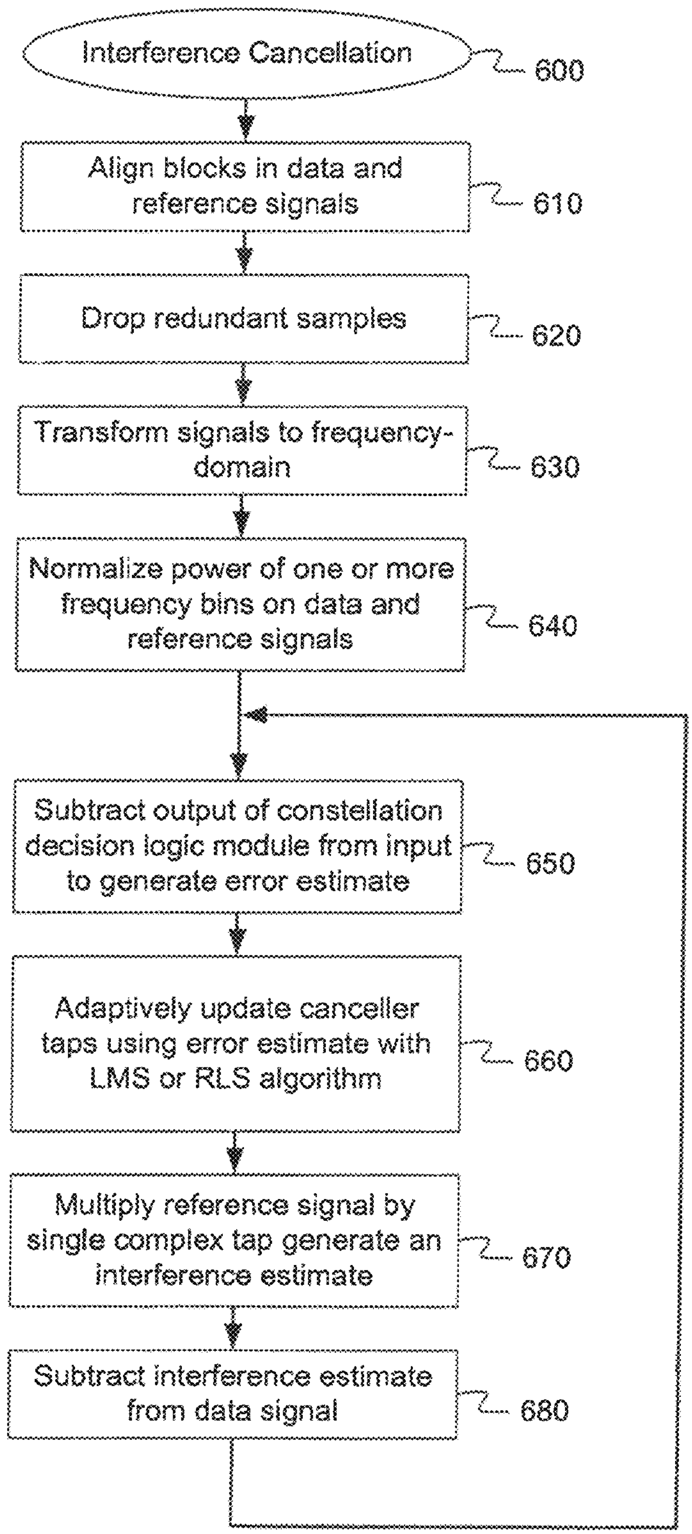

Interference Cancellation
600
Align blocks in data and reference signals
610
Drop redundant samples
620
Transform signals to frequency-domain
630
Normalize power of one or more frequency bins on data and reference signals
640
Subtract output of constellation decision logic module from input to generate error estimate
650
Adaptively update canceller taps using error estimate with LMS or RLS algorithm
660
Multiply reference signal by single complex tap generate an interference estimate
670
Subtract interference estimate from data signal
680

Figure 6

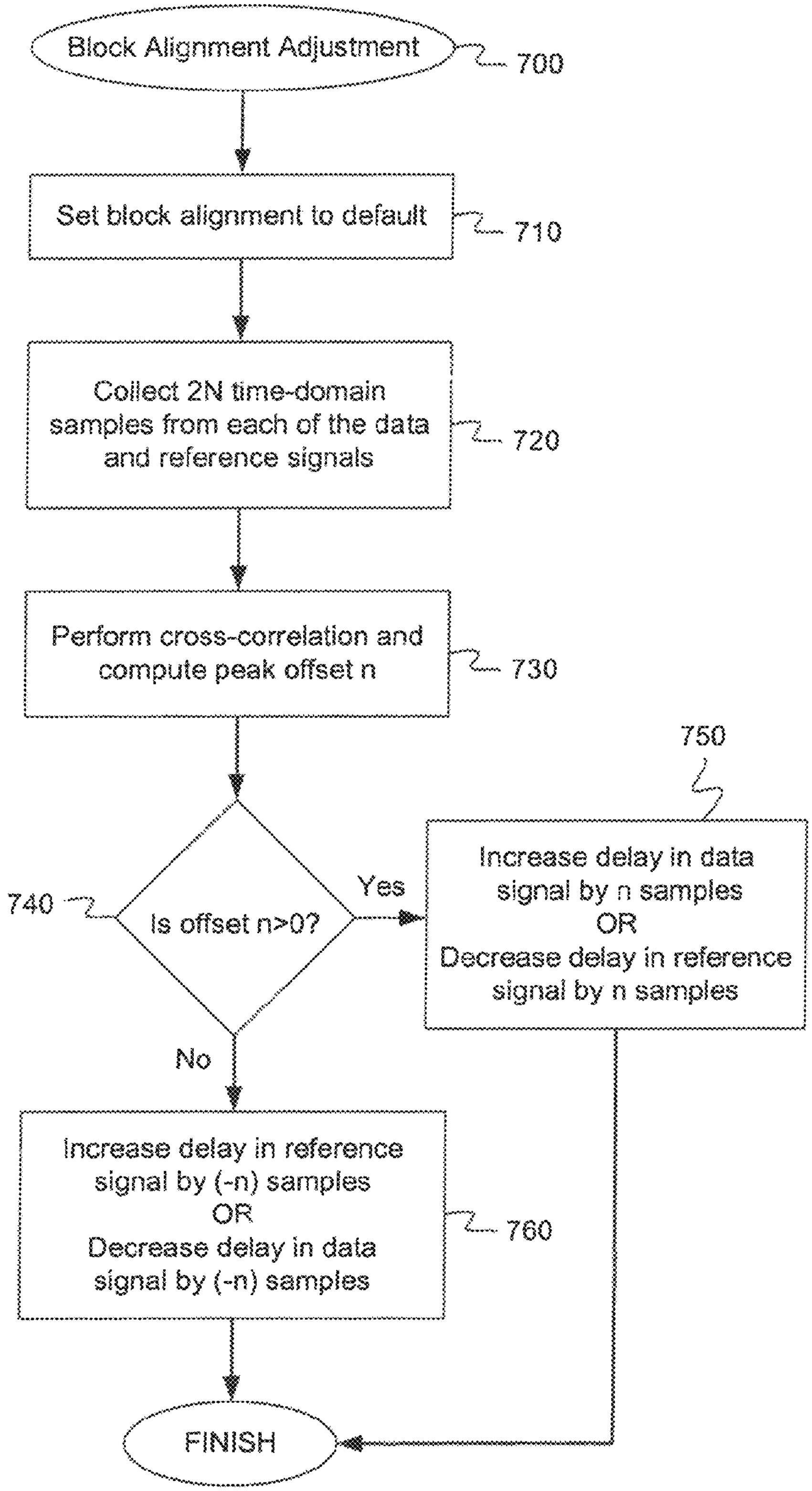

Block Alignment Adjustment
700
Set block alignment to default
710
Collect 2N time-domain samples from each of the data and reference signals
720
Perform cross-correlation and compute peak offset n
730
750
740
Is offset n>0?
Yes
Increase delay in data signal by n samples
OR
Decrease delay in reference signal by n samples
No
Increase delay in reference signal by (-n) samples
OR
Decrease delay in data signal by (-n) samples
760
FINISH

Figure 7

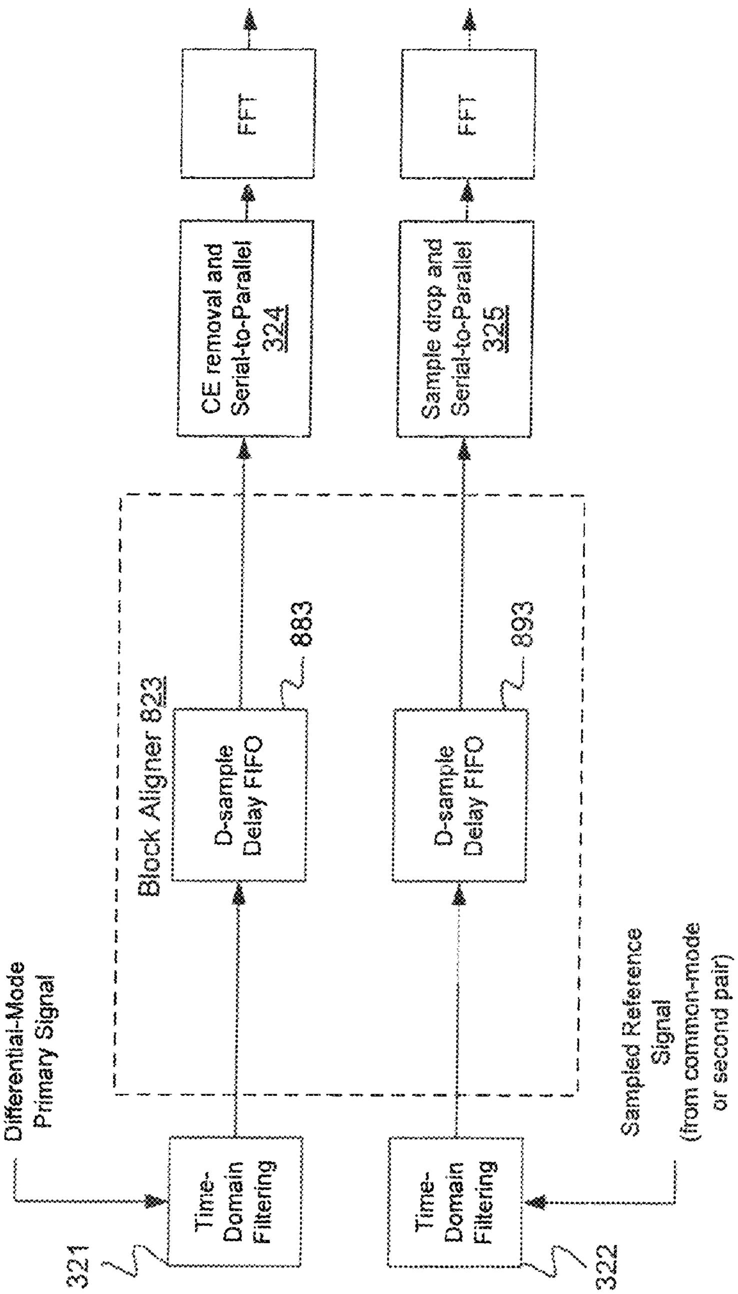

Sampled Differential-Mode Primary Signal
321
Time-Domain Filtering
Block Aligner 823
D-sample Delay FIFO
883
CE removal and Serial-to-Parallel 324
FFT
322
Time-Domain Filtering
Sampled Reference Signal (from common-mode or second pair)
D-sample Delay FIFO
893
Sample drop and Serial-to-Parallel 325
FFT

Figure 8

ADAPTIVE FREQUENCY-DOMAIN REFERENCE NOISE CANCELLER FOR MULTICARRIER COMMUNICATIONS SYSTEMS

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. application Ser. No. 12/287,577, filed Oct. 10, 2008, assigned U.S. Pat. No. 8,605,837, which is hereby incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to a multi-carrier communication system and, in particular, to noise cancellation in a multi-carrier communication system.

2. Background Art

A multi-carrier communication system, such as a Discrete Multi-Tone (DMT) system in the various types of Digital Subscriber Line (DSL), for example, asymmetric digital subscriber line (ADSL) and very high-speed digital subscriber line (VDSL) systems, carries an information bit stream from a transmitter to a receiver. The information bit stream is typically converted into a sequence of data symbols having a number of tones. Each tone may be a group of one or more frequencies defined by a center frequency and a set bandwidth. The tones are also commonly referred to as sub-carriers or sub-channels. Each tone acts as a separate communication channel to carry information between a local transmitter-receiver (transceiver) device and a remote transceiver device.

BRIEF SUMMARY OF THE INVENTION

FIG. **1** is a block diagram illustrating a conventional DMT receiver. A channel equalizer is used to control the spread of the data symbols after going through the channel A cyclic prefix (CP) may be employed in such systems to simplify channel equalization to minimize a source of cross channel interference. Generally, if the length of the channel impulse response is equal to or less than the cyclic prefix length plus one sample, then channel equalization is trivial and perfect equalization can be achieved. The channel can be inverted in the frequency domain after a discrete Fourier transform (DFT) by a single complex multiply for each sub-channel. This is usually referred to as frequency-domain equalization (FEQ).

On transmission lines in DMT communication systems, such as ADSL or VDSL, the data signal is generally transmitted differentially. Interference such as radio-frequency interference (RFI), crosstalk and impulse noise electromagnetically couples into both the common mode and the differential mode of such transmission lines. In the case of a binder containing multiple transmission lines, such interference may couple into some or all of the transmission line in the binder and such noise may be correlated between lines.

Conventional techniques for reducing differential noise, thereby improving data rates over the DSL, include use of common-mode information. In a traditional DSL system, the common-mode voltage is measured, an estimate of the differential-mode interference is constructed and the interference estimate is subtracted from the desired signal.

Traditional cancellation may occur in the time-domain or the frequency domain. For example, frequency bands containing RFI are band-pass filtered and then subtracted from the differential-mode signal in the time domain. In the frequency domain, a small set of frequency bins are used to compute and remove an estimate of RFI on a larger number of data carrying frequency bins. Other conventional systems cancel crosstalk in both the time domain and the frequency domain by solving a specific set of equations.

However, there are significant drawbacks associated with filtering and subtracting an interference estimate in the time-domain. For example, training and updating the noise estimation unit is difficult, especially in the presence of a data signal. Furthermore, time-domain subtraction tends to result in noise enhancement. A reduction in the power spectral density (PSD) of the interference may be achieved over parts of the frequency band where the interference is strongest, but interference PSD enhancement may occur in other frequency regions, resulting in sub-optimal system performance.

Known frequency-domain techniques also have significant limitations. Common-mode interference may not be limited to crosstalk or RFI alone, but may be a combination of the two. There may also be wideband noise from sources other than radio transmitters (RFD or other communications systems (crosstalk) that is correlated between the common and differential modes. Conventional solutions are suited to target only crosstalk or RFI; not both. Also, the interference sources and their associated coupling transfer functions will, in general, change over time. Known cancellers do not have the ability to adapt to these changing conditions in the presence of the data signal. Furthermore, in a practical implementation, there are complications and difficulties associated with the dynamic range of both the differential-mode and common-mode signals. In implementations in which the multi-carrier communications system is an ADSL or VDSL system, there may be further complications involving interaction of the canceller with On-Line Reconfiguration (OLR), Seamless Rate Adaptation (SRA), and bitswap as defined in the various ADSL and VDSL standards. During such events the transmitted power and/or the constellation size changes for one or more sub-carriers.

BRIEF DESCRIPTION OF THE DRAWINGS/FIGURES

The present invention is illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings.

FIG. **1** is a block diagram illustrating a conventional DMT receiver.

FIG. **2** is a block diagram illustrating an embodiment of a discrete multi-tone system.

FIG. **3** is a block diagram illustrating one embodiment of a receiver having an adaptive frequency-domain reference noise canceller.

FIG. **4** is a block diagram illustrating an alternative embodiment of a receiver having an adaptive frequency-domain reference noise canceller.

FIG. **5** is a block diagram illustrating a second alternative embodiment of a receiver having an adaptive frequency-domain reference noise canceller.

FIG. **6** is a flow chart illustrating one embodiment of an interference cancellation method.

FIG. **7** is a flow chart illustrating one embodiment of a block alignment adjustment method.

FIG. **8** is a block diagram illustrating one embodiment of a block aligner.

DETAILED DESCRIPTION OF THE INVENTION

In the following description, numerous specific details are set forth, such as examples of specific commands, named components, connections, number of frames, etc., in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well known components or methods have not been described in detail but rather in a block diagram in order to avoid unnecessarily obscuring the present invention. Thus, the specific details set forth are merely exemplary. The specific details may be varied from and still be contemplated to be within the scope of the present invention.

Some portions of the description that follow are presented in terms of algorithms and symbolic representations of operations on data that may be stored within a memory and operated on by a processor. These algorithmic descriptions and representations are the means used by those skilled in the art to effectively convey their work. An algorithm is generally conceived to be a self-consistent sequence of acts leading to a desired result. The acts are those requiring manipulation of quantities. Usually, though not necessarily, these quantities take the form of electrical or magnetic signals capable of being stored, transferred, combined, compared, and otherwise manipulated. It has proven convenient at times, principally for reasons of common usage, to refer to these signals as bits, values, elements, symbols, characters, terms, numbers, parameters, or the like.

The following detailed description includes several modules, which will be described below. These modules may be implemented by hardware components, such as logic, or may be embodied in machine-executable instructions, which may be used to cause a general-purpose or special-purpose processor programmed with the instructions to perform the operations described herein. Alternatively, the operations may be performed by a combination of hardware and software.

Embodiments of a method and apparatus are described to cancel interference in a multi-carrier communications system. In one embodiment, a data signal and a reference signal are received at a receiver. The reference signal is obtained by measuring a common-mode or differential-mode voltage. A block aligner is used to align data blocks in the data and reference signals to increase cross-correlation between the data signal and the reference signal as compared to the unaligned data and reference signals. The aligned time-domain signals are transformed to the frequency-domain where interference cancellation occurs. A tone-by-tone canceller includes a decision feedback mechanism to adapt the canceller under changing conditions in the presence of the data signal in the frequency-domain.

FIG. **2** is a block diagram illustrating an embodiment of a discrete multi-tone system. The discrete multi-tone system **200**, such as a Digital Subscriber Line (DSL) based network, may have two or more transceivers **202** and **204**, such as a DSL modem in a set top box. In one embodiment, the set top box may be a stand-alone DSL modem. In one embodiment, for example, the set top box employs a DSL modem along with other media components to combine television (Internet Protocol TV or satellite) with broadband content from the Internet to bring the airwaves and the Internet to an end user's TV set. Multiple carrier communication channels may communicate a signal to a residential home. The home may have a home network, such as an Ethernet. The home network may either use the multiple carrier communication signal directly, or convert the data from the multiple carrier communication signal. The set top box may also include, for example, an integrated Satellite and Digital Television Receiver, High-Definition Digital Video Recorder, Digital Media Server and other components.

The first transceiver **202**, such as a Discrete Multi-Tone transmitter, transmits and receives communication signals from the second transceiver **204** over a transmission medium **206**, such as a telephone line. Other devices such as telephone **208** may also connect to this transmission medium **206**. An isolating filter **210** generally exists between the telephone **208** and the transmission medium **206**. A training period occurs when initially establishing communications between the first transceiver **202** and a second transceiver **204**.

The discrete multi-tone system **200** may include a central office, multiple distribution points, and multiple end users. The central office may contain the first transceiver **202** that communicates with the second transceiver **204** at an end user's location.

Each transmitter portion **217**, **219** of the transceivers **202**, **204**, respectively, may transmit data over a number of mutually independent sub-channels i.e., tones. In a DMT communication system, data samples on each tone are represented as one of a set of finite number of points in a two-dimensional (2D) Quadrature Amplitude Modulation (QAM) constellation. The transmitted data in a multi-carrier system is usually represented by a point from a constellation of a finite set of possible data points, regularly distributed over a two dimensional space. Each sub-channel carries only a certain portion of data through QAM of the sub-carrier. The number of information bits loaded on each tone and the size of corresponding QAM constellation may potentially vary from one tone to another and depend generally on the relative power of signal and noise at the receiver. When the characteristics of signal and noise are known for all tones, a bit-loading algorithm may determine the optimal distribution of data bits and signal power amongst sub-channels. Thus, a transmitter portion **217**, **219** of the transceivers **202**, **204** modulates each sub-carrier with a data point in a QAM constellation.

It should be noted that embodiments of the present invention are described below in reference to receiver **316**, which represents one embodiment of receiver **216**, for ease of discussion, and that receiver **218** may operate in a similar manner as described below for receiver **316**.

FIG. **3** is a block diagram illustrating one embodiment of a receiver having an adaptive frequency-domain reference noise canceller. In this embodiment, receiver **316** includes time domain filtering modules **321**, **322**, block aligner **323**, cyclic extension (CE) removal and serial-to-parallel module **324**, sample drop and serial-to-parallel module **325**, fast Fourier transform (FFT) modules **326**, **327**, channel flattening frequency-domain equalizer (CF-FEQ) module **328**, bin power normalization module **329**, adders **330**, **333**, interference estimator module **331**, gain inversion and constellation scaling (GICS) module **332**, and constellation decision logic module **334**. Additional modules and functionality may exist in the receiver **316** that are not illustrated so as not to obscure an understanding of embodiments of the present invention. It should be noted that the operations of one or more modules may be incorporated into or integrated with other modules.

In one embodiment, receiver **316** is implemented in a DMT communications system operating over a twisted-pair communications channel. N is a variable representing the number of tones used in the multi-carrier communication receiver. The communications system may operate in the presence of RFI, crosstalk and other interference. In this embodiment, received samples of a differential-mode primary data signal sent over the twisted pair are provided to a first time-domain filtering module **321**. Additionally, a sampled reference signal is received and provided to a second time-domain filtering module **322**. The reference signal is obtained by sampling the common-mode signal of the same twisted-pair as the primary data signal. In an alternative embodiment, the reference signal is obtained by sampling the differential mode interference from a second twisted-pair that is not used for data transmission. In another alternative embodiment, the primary data signal is obtained by sampling the differential voltage of a copper pair in a twisted copper quad and the reference signal is obtained by sampling the differential-mode interference from the other two wires of the twisted quad.

In this embodiment, receiver **316** is configured to operate independently of the source of the reference signal. A data signal and a reference signal are received and undergo digital time-domain filtering at modules **321** and **322** respectively. Receiver **316** further includes a block aligner module **323**. Block aligner module **323** adjusts the relative alignment of the 2N-sample blocks of the primary data signal and the reference signal as needed. The block aligner module **323** may be implemented with sample-dropping capability, by programming delay First in, First out (FIFO) buffers, or by adjusting the group delay of programmable finite impulse response (FIR) filters. The block aligner module **323** aligns the blocks such that the cross correlation of the reference signal and the primary line interference signal is increased as compared to the cross correlation of the unaligned data and reference signals. For example, the increase in cross-correlation may be in a range of approximately 50 percent to over an order of magnitude. In one embodiment, the blocks are aligned such that the cross-correlation is maximized. Block aligner module **323** will be described further below, with respect to FIG. **8**.

A first output of block aligner module **323** provides the aligned data signal to cyclic extension (CE) removal and serial-to-parallel module **324**. A second output of block aligner module **323** provides the aligned reference signal to sample drop and serial-to-parallel module **325**. Modules **324** and **325** serve to remove samples corresponding to any cyclic extension that may have been added to the data stream at the transmitter as well as convert the serial sample stream in to chunks which may be operated on in parallel.

The data signal and reference signal undergo 2N-point discrete Fourier transforms (DFT). In this embodiment, the DFT is computed efficiently by means of a fast Fourier transform (FFT) at FFT modules **326** and **327**. The time-domain samples of both the data signal and the reference signal are provided to FFT modules **326** and **327** which convert the samples into frequency-domain symbols to be used by the canceller.

The output of FFT module **326** for the data signal is sent to a channel flattening frequency-domain equalizer (CF-FEQ) module **328**. The CF-FEQ module normalizes the phase and power on each frequency bin of the data signal. In a traditional DMT system, at the output of the FFT, each frequency bin of the data signal undergoes an FEQ multiply that inverts the channel attenuation and phase rotation, inverts the fine gain adjustment value assigned to the bin, and adjusts for the constellation size. The result is such that the FEQ output is scaled to an integer grid for decoding. In this embodiment of the present invention, the traditional FEQ is split into a CF-FEQ module **328** and a gain inversion and constellation scaling (GICS) module **332**. The two stage approach allows the data signal from the output of FFT module **326** to be normalized for computationally efficient removal of interference using integer arithmetic. It also decouples on-line reconfiguration (OLR), seamless rate adaptation (SRA) and bitswap from the reference noise canceller. That is, the reference noise canceller taps do not need to change during or after such an event.

The output of FFT module **327** for the reference signal undergoes a scaling stage in which the power on each frequency bin of the reference signal is normalized. The bin-power normalization module **329** receives the output of FFT module **327** and corrects amplitude and phase distortion in the reference signal. The bin-power normalization module **329** produces a normalized reference channel output signal Yref.

The normalized reference channel output signal Yref is provided to an interference estimator module **331**. Interference estimator module **331** multiplies the reference signal Yref by a single complex tap for each frequency bin thus forming an estimate of the interference in the differential-mode signal for each bin. This estimate is subtracted from the normalized primary channel output signal Y provided by the CF-FEQ module **328**. The subtraction is performed by adder **330** and results in a canceller output signal Yc. The canceller output signal Yc is provided to an input of the GICS module **332**.

GIGS module **332** adjusts the signal for per-bin gain and constellation size. The GIGS module **332** produces an output signal. Xhat which is provided to an input of a constellation decision logic module **334**. In the constellation decision logic module **334**, the signal Xhat undergoes constellation decoding where constellation decisions are formed. The constellation decision logic module **334** may include a trellis decoder or a simple un-coded constellation decoder or slicer. Constellation decision logic module **334** produces a constellation decision signal X. The constellation decision signal X is subtracted from the GICS module output signal Xhat to form a decision error estimate E. The subtraction is performed by adder **333**. The decision error estimate E is used to adaptively update the canceller taps in the interference estimator module **331**. In one embodiment, a least-mean-square (LMS) algorithm is used to update the taps. In alternative embodiments, other algorithms may be used to update the taps such as a recursive least square (RLS) algorithm, a gradient computation, or other algorithm. The structure of receiver **316** allows the canceller to adapt under changing conditions, such as interference sources and their associated coupling transfer functions, and effectively cancel interference in the presence of the actual data signal.

FIG. **4** is a block diagram illustrating an alternative embodiment of a receiver **416** having an adaptive frequency-domain reference noise canceller. In this embodiment, the CF-FEQ module **328** of FIG. **3** is removed and the GIGS module **332** of FIG. **3** is replaced with FEQ module **435**. FEQ module **435** receives the canceller output signal Yc at an input and provides the decoder input signal Xhat to constellation decision logic module **334**. The canceller output signal Yc is obtained by subtracting the interference estimate directly from the primary channel output Y of FFT module **326**. The reference signal is processed in the same manner as described above with respect to FIG. **3**.

FIG. **5** is a block diagram illustrating a second alternative embodiment of a receiver having an adaptive frequency-domain reference noise canceller. In this embodiment, the CF-FEQ module **328** of FIG. **3** is replaced with FEQ module **536** and GICS module **332** of FIG. **3** is removed. FEQ module **536** receives the output of FFT module **326** at an input and provides an FEQ output signal Y to adder **330**. Bin power normalization module **329** of FIG. **3** has also been removed in this embodiment. The reference channel output Yref of the FFT module **327** is directly multiplied by a single complex tap to form an interference estimate at interference estimator module **331**. The interference estimate is subtracted from the

FEQ output signal Y at adder **330** and the canceller output Y is provided directly to the constellation decision logic module **334**.

FIG. **6** is a flow chart illustrating one embodiment of an interference cancellation method **600**. The process **600** may be performed by processing logic that comprises hardware, firmware, software, or a combination thereof. In one embodiment, process **600** is performed by the receiver **316** of FIG. **3**.

Referring to FIG. **6**, interference cancellation method **600** reduces the interference in a data signal in a multi-carrier communications system. At block **610**, method **600** aligns data blocks from a received data signal and a reference signal to increase cross correlation between the data signal and the reference signal as compared to the unaligned data and reference signals. The block alignment process will be discussed further below with respect to FIG. **7**.

At block **620**, method **600** drops unneeded samples corresponding to the cyclic extension of the data signal from the aligned data and reference signals. Method **600** also removes any cyclic extension that may have been added to the data stream at the transmitter as well as converts the serial sample stream in to chunks which may be operated on in parallel. At block **630**, method **600** transforms the data and reference signals from the time-domain to the frequency-domain. The transformation may be accomplished with the use of a discrete Fourier transform (DFT). In one embodiment, the DFT is performed by FFT modules **326** and **327** of FIG. **3**.

At block **640**, method **600** normalizes the power on each frequency bin of the data and reference signals. Method **600** corrects any amplitude and phase distortion in the signal to enable efficient noise cancellation. At block **650**, the data signal undergoes a constellation decision logic stage where constellation decisions are formed. The output of the constellation decision logic is subtracted from the input to form an error estimate. The error estimate is used to adaptively update canceller taps at block **660**. In one embodiment, a least-mean-square (LMS) algorithm is used to update the taps. In alternative embodiments, other algorithms may be used to update the taps such as a recursive least square (RLS) algorithm, a gradient computation, or other algorithm.

At block **670**, method **600** multiplies the transformed reference signal by a single complex tap for each of one or more frequency bins of the reference signal. The multiplication results in an estimate of the interference in the data signal. At block **680**, method **600** subtracts the interference estimate from the data signal. The subtraction results in a canceller output signal which is then applied to an input the constellation decision logic and method **600** continues at block **650** with the new input. In this manner, method **600** is able to adaptively update the interference canceller with an interference estimate to cancel changing sources of interference during data transmission.

FIG. **7** is a flow chart illustrating one embodiment of a block alignment adjustment method **700**. The process **700** may be performed by processing logic that comprises hardware, firmware, software, or a combination thereof. In one embodiment, process **700** is performed by the block aligner **323** of FIG. **3**.

Referring to FIG. **7**, block alignment adjustment method **700** enables alignment of data blocks from at least a received data signal and a reference signal to increase cross correlation between the data signal and the reference signal as compared to the unaligned data and reference signals. Alignment of the data blocks allows for the canceller to achieve optimal noise cancellation. At block **710**, method **700** sets the block alignment to a default value. In one embodiment, the default value may be zero offset in both the data signal and the reference signal.

At block **720**, method **700** collects 2N time-domain samples from each of the time domain signal and the reference signal. In one embodiment, the collection of each of the two sets of 2N samples begins at the same absolute time. This results in the 2N-sample blocks of the data signal and reference signal being roughly-aligned.

At block **730**, method **700** performs cross-correlation of the data and reference signals and computes a peak offset value. Block alignment fine tuning is performed by using the cross-correlation of the interference on the data and reference signals. The measurement occurs when the data signal is not present, such as before modem training commences or at a time during modem training when the far-end transmitter is quiet. After dual 2N-sample blocks are captured at block **720**, the cross correlation is computed as

$$(y^*y_{ref})[n]=\Sigma_j y[j]^*y_{ref}^*[n+j] \tag{1}$$

where y is a block of 2N samples from the data signal in the time-domain during a quiet period, y_{ref} is the corresponding block of 2N samples from the reference signal in the time-domain during the same time period, n is the peak offset between the data and reference signals and j is a counting index. The offset is found by determining the values of n for which the cross correlation $(y^*y_{ref})[n]$ is greater than when there is no offset (i.e. n=0). In one embodiment method **700** may determine the value of n for which the cross correlation is a maximum. A range of values for n may result in increased cross correlation, however as the values become nearer the value which results in maximum cross-correlation, the efficiency of the interference cancelling increases. Method **700** selects one value of n to use as the offset in the block aligner.

At block **740**, method **700** makes a determination as to whether the selected value of n is greater or less than zero. If n is greater than zero, method **700** proceeds to block **750**. At block **750**, method **700** adjusts the block alignment by the offset n samples. In one embodiment, method **700** increases the delay in the data signal by n samples and in an alternative embodiment, method **700** decreases the delay in the reference signal by n samples. If n is less than zero, method **700** proceeds to block **760**. At block **760**, method **700** adjusts the block alignment by the offset, n samples. In one embodiment, method **700** increases the delay in the reference signal by (−n) samples and in an alternative embodiment, method **700** decreases the delay in the data signal by (−n) samples. After the block alignment has been adjusted at either block **750** or **760**, method **600** ends.

FIG. **8** is a block diagram illustrating one embodiment of a block aligner **823**. The block aligner **823** includes two D-sample delay FIFO buffers **883**, **893**. A first FIFO buffer **883** is in the primary data signal path and a second FIFO buffer **893** is in the reference signal path. If the delay through both time-domain filtering blocks **321**, **322** is equivalent, and the Serial-to-Parallel blocks **324**, **325** are synchronized such that sample collection for each block begins at the same time on both channels, then the block aligner **823** in this form allows for a plus or minus D-sample fine-tuning delay adjustment between the primary and reference paths. In an alternative embodiment, finite impulse response (FIR) filters are used in place of FIFO buffers **883**, **893**. Block aligner **823** aligns the blocks of the data and reference signals such that there is an increase in the cross-correlation between the data signal and the reference signal as compared to the unaligned data and reference signals.

In one embodiment, the methods described above may be embodied onto a machine-readable medium. A machine-readable medium includes any mechanism that provides (e.g., stores and/or transmits) information in a form readable by a machine (e.g., a computer). For example, a machine-readable medium includes read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; DVD's, or any type of media suitable for storing electronic instructions. The information representing the apparatuses and/or methods stored on the machine-readable medium may be used in the process of creating the apparatuses and/or methods described herein.

While some specific embodiments of the invention have been shown the invention is not to be limited to these embodiments. The invention is to be understood as not limited by the specific embodiments described herein, but only by the scope of the appended claims.

What is claimed is:

1. A block aligner for aligning a data block in a data signal with a data block in a reference signal, the block aligner comprising:
- a first buffer configured to:
  - receive the data signal,
  - initiate a first tuning on the data signal if a delay between the data signal and the reference signal is equivalent; and
- a second buffer configured to:
  - receive the reference signal, and
  - initiate a second tuning on the reference signal if the delay between the data signal and the reference signal is equivalent.

2. The block aligner of claim **1**, wherein the first buffer and the second buffer are first-in-first-out (FIFO) buffers.

3. The block aligner of claim **1**, wherein the first buffer and the second buffer are D-sample delay FIFO buffers.

4. The block aligner of claim **1**, wherein the first buffer is configured to initiate the first tuning on the data signal to change a cross-correlation between the data signal and the reference signal.

5. The block aligner of claim **1**, wherein the second buffer is configured to initiate the second tuning on the reference signal to change a cross-correlation between the data signal and the reference signal.

6. The block aligner of claim **1**, further comprising:
- a first time domain filtering block coupled to the first buffer, wherein the first time domain filtering block is configured to send the data signal to the first buffer; and
- a second time domain filtering block coupled to the second buffer, wherein the second time domain filtering block is configured to send the reference signal to the second buffer.

7. The block aligner of claim **1**, further comprising:
- a first serial-to-parallel block coupled to the first buffer, wherein the first buffer is further configured to send a tuned data signal to the first serial-to-parallel block; and
- a second serial-to-parallel block coupled to the second buffer, wherein the second buffer is further configured to send a tuned reference signal to the second serial-to-parallel block.

8. The block aligner of claim **7**, wherein the first serial-to-parallel block and the second serial-to-parallel block are synchronized such that sample collection of the first serial-to-parallel block and the second serial-to-parallel block begins at a same time.

9. The block aligner of claim **1**, wherein the first buffer is further configured to:
- initiate cancelling interference in the data signal based on the first tuning.

10. The block aligner of claim **1**, wherein the second buffer is further configured to:
- initiate cancelling interference in the reference signal based on the second tuning.

11. A block alignment adjustment method, comprising:
- collecting, using a receiver device, a plurality of first samples from a data signal;
- collecting, using the receiver device, a plurality of second samples from a reference signal;
- cross-correlating, using the receiver device, the plurality of first samples and the plurality of second samples; and
- cancelling, using the receiver device, interference in the plurality of first samples and the plurality of second samples by tuning the plurality of first samples and the plurality of second samples based on the cross-correlating.

12. The block alignment adjustment method of claim **11**, wherein the plurality of first samples and the plurality of second samples are collected simultaneously.

13. The block alignment adjustment method of claim **11**, further comprising:
- computing a peak offset value based on the cross-correlating.

14. An apparatus, comprising:
- a receiver configured to receive a plurality of first samples from a data signal and a plurality of second samples from a reference signal; and
- a block aligner, coupled to the receiver, configured to:
  - cross-correlate the plurality of first samples and the plurality of second samples, and
  - cancel interference in the plurality of first samples and the plurality of second samples by tuning the plurality of first samples and the plurality of second samples based on the cross-correlated plurality of first samples and plurality of second samples.

15. The apparatus of claim **14**, wherein the plurality of first samples and the plurality of second samples are collected simultaneously.

16. The apparatus of claim **14**, wherein the block aligner is further configured to compute a peak offset value based on the cross-correlating.

17. The apparatus of claim **14**, further comprising:
- a first buffer configured to initiate a first tuning on the data signal if a delay between the data signal and the reference signal is equivalent; and
- a second buffer configured to initiate a second tuning on the reference signal if the delay between the data signal and the reference signal is equivalent.

18. The apparatus of claim **17**, wherein the first buffer is configured to initiate the first tuning on the data signal to change a cross-correlation between the data signal and the reference signal.

19. The apparatus of claim **17**, wherein the second buffer is configured to initiate the second tuning on the reference signal to change a cross-correlation between the data signal and the reference signal.

20. The apparatus of claim **14**, wherein the block aligner is further configured to align the plurality of first samples and the plurality of second samples such that cross-correlation between the plurality of first samples and the plurality of second samples is maximized.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 9,160,381 B2
APPLICATION NO. : 14/099763
DATED : October 13, 2015
INVENTOR(S) : Wiese et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Specification:
In column 6, line 21, replace “GIGS” with --GICS--.
In column 6, line 22, replace “GIGS” with --GICS--.
In column 6, line 47, replace “GIGS” with --GICS--.

Signed and Sealed this
Twenty-fifth Day of October, 2016

Michelle K. Lee

Michelle K. Lee
Director of the United States Patent and Trademark Office